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MULTI-CHIPS STACKED PACKAGE

BACKGROUND OF THE INVENTION

Field of Invention

[0001] This invention relates to a multi-chips stacked package having a heat spreader and a dam therein. More particularly, the present invention is related to a multi-chips stacked package with a dam that is utilized for enclosing the underfill which covers the upper surface of the substrate and encloses an upper chip and a lower chip so as to prevent the underfill from bleeding and have the underfill connected to the substrate and the heat spreader in a suitable manner. Thus, the electrically conductive bumps connecting the substrate and the upper chip will be prevented from being damaged due to lower the stress at the electrically conductive bumps.

Related Art

[0002] As we know, in the semiconductor industries, the manufacture of semiconductors mainly comprises the manufacture of wafers and the assembly of integrated circuits devices. Therein, the integrated circuits (ICs) devices are completely formed by the processes of forming integrated circuits devices on the semiconductor wafers, sawing the wafers into individual integrated circuits devices, placing the individual integrated circuits devices on the substrates, electrically connecting the integrated circuits devices to the substrates and encapsulating the integrated circuits devices and substrates to form a plurality of assembly packages. Due to the encapsulation covering the integrated circuits devices, the integrated circuits devices are able to be protected from the damp entering. In addition, the assembly packages may further provide external terminals for connecting to printed

circuit board (PCB).

[0003] However, recently, integrated circuits packaging technology is becoming a limiting factor for the development in packaging integrated circuits devices of higher performance. Semiconductor package designers are struggling to keep pace with the increase in pin count, size limitations, low profile, and other evolving requirements for packaging and mounting integrated circuits.

[0004] Due to the assembly package in miniature and the integrated circuits operation in high frequency, MCM (multi-chips module) packages are commonly used in said assembly packages and electronic devices. Usually, said MCM package mainly comprises at least two chips encapsulated therein, for example a processor unit, a memory unit and related logic units, so as to upgrade the electrical performance of said assembly package. In addition, the electrical paths between the chips in said MCM package are short so as to reduce the signal delay and save the reading and writing time.

[0005] Per the above-mentioned, a multi-chips stacked package is provided, as shown in FIG.1, as a standard and common design. Referring to FIG. 1, it is characterized that an upper chip 110 is flipped over and disposed above an opening 122 passing through the upper surface 124 and the lower surface 126 of the substrate 120 and a lower chip 130 is accommodated in the opening 122 and electrically connected to the upper chip 110 through electrically conductive bumps 170. Generally speaking, the upper chip 110 and the lower chip 130 are a memory chip and a logic chip respectively. In such a manner, the electrical signals are able to be integrated in the package and then are transmitted to external devices through solder balls 128 attached to the lower surface 126 of the substrate 120. Accordingly, the size of said multi-chips stacked package is reduced and the transmission path of the electrical

signals are shortened. Namely, the signal delay is reduced and the electrical performance of said multi-chips stacked package is upgraded.

[0006] As mentioned above and per the conventional invention as shown in FIG. 1, the upper chip 110 is electrically connected to the substrate 120 through electrically conductive bumps 170. Generally, the organic substrate, for example Bismaleimide-Triazine (BT), is taken as the substrate 120 to carry the upper chip 110 wherein the coefficient of thermal expansion of the substrate120 is about $16*10^{-6}$ ppm/℃ and the coefficient of thermal expansion of the upper chip 110 is about $4*10^{-6}$ ppm/℃. Accordingly, the coefficient of thermal expansion of the upper chip 110 is much smaller than that of the substrate 120 and the electrically conductive bumps 170 connecting the upper chip 110 and the substrate 120 are usually damaged due to the CTE mismatch of the substrate 120 with the upper chip 110. Notwithstanding, there is an underfill 160 interposed between the upper chip 110 and the substrate 120 and filled into the space between the upper chip 110 and the substrate 120 to lower the stress at the electrically conductive bumps 170, the bumps 170 are still damaged due to the much difference of the coefficient of thermal expansion of the substrate 120 from that of the upper chip 110.

[0007] Therefore, providing another multi-chips stacked package to solve the mentioned-above disadvantages is the most important task in this invention.

SUMMARY OF THE INVENTION

[0008] In view of the above-mentioned problems, an objective of this invention is to provide a multi-chips stacked package which is characterized in that the electrically conductive bumps provided in the multi-chips stacked package is able to be prevented

from being damaged due to a reinforced structure made of the underfill, the heat spreader and the dam.

[0009] To achieve the above-mentioned objective, a multi-chips stacked package is provided, wherein the multi-chips stacked package mainly comprises a substrate having an opening, an upper chip, a lower chip, a heat spreader, a dam, a plurality of electrically conductive bumps and an underfill. Therein, the upper chip is flipped over and disposed above the opening, and the active surface of the upper chip is attached to the upper surface of the substrate through the electrically conductive bumps; the lower chip is accommodated in the opening and connected to the upper chip by another electrically conductive bumps; and the heat spreader is attached to the back surface of the upper chip. Moreover, the dam is disposed on the substrate and below the heat spreader, and connected to the heat spreader; and the underfill is filled in a space enclosed by the dam, the upper surface of the substrate and the heat spreader so as to have the underfill connected to the heat spreader, the dam and the substrate in a suitable manner. Accordingly, a reinforced structure, is formed by the heat spreader, the underfill and the dam, lowers the stress at the electrically conductive bumps connecting the upper chip and the substrate and to prevent the electrically conductive bumps from being damaged.

[0010] In summary, this invention is related to a multi-chips stacked package utilizing a dam for enclosing the underfill which covers the upper surface of the substrate and encloses the upper chip and the lower chip so as to prevent the underfill from bleeding and have the underfill connected to the substrate and the heat spreader in a suitable manner. Thus, the stress at the electrically conductive bumps interposed between the upper chip and the substrate will be lowered. In such a manner, the electrically conductive bumps connecting the substrate and the upper chip will be

prevented from being damaged. As mentioned above, the underfill is connected to the heat spreader, the dam and the substrate so as to restrain the warpage of the substrate and the deformation of the upper chip. Moreover, when the coefficient of the thermal expansion of the heat spreader be substantially the same as the substrate is provided, for example a dummy chip, the substrate and the heat spreader with higher stiffness and much rigidity will be regarded as covers to have the upper chip to be interposed between the heat spreader and the substrate to form a sandwich beam structure. Accordingly, the underfill is regarded as a core layer and able to absorb a lot of stress energy and the shear stress at the electrically conductive bumps connecting the substrate and the upper chip. Thus, the substrate is prevented from being warped so that the reliability of the multi-chips stacked package will be upgraded. Moreover, the heat spreader is mounted on the back surface of the upper chip so that the thermal performance of the multi-chips stacked package will be enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The invention will become more fully understood from the detailed description given herein below illustrations only, and thus are not limitative of the present invention, and wherein:

[0012] FIG. 1 is a cross-sectional view of the conventional multi-chips stacked package;

[0013] FIG. 2 is a cross-sectional view of a multi-chips stacked package according to the preferred embodiment;

[0014] FIG. 3 is a cross-sectional view along line AA' of the multi-chips stacked package shown in FIG. 2; and

[0015] FIG. 4 is a cross-sectional view of a multi-chips stacked package according to another preferred embodiment.

DETAILED DESCRIPTION OF THE INVENTION

[0016] The multi-chips stacked package according to the preferred embodiments of this invention will be described herein below with reference to the accompanying drawings, wherein the same reference numbers refer to the same elements.

[0017] In accordance with a preferred embodiment as shown in FIG. 2, there is provided a multi-chips stacked package. Referring to FIG. 2, the multi-chips stacked package mainly comprises an upper chip 210, a substrate 220 having an opening 222, a lower chip 230, a dam 240, a heat spreader 250, an underfill 260, a plurality of first electrically conductive bumps 270, and a plurality of second electrically conductive bumps 280. Therein, the substrate 220 further has an upper surface 224 and a lower surface 226, and the opening 222 passes through the upper surface 224 and the lower surface 226. Besides, the upper chip 210 is flipped over and attached on the upper surface 224 of the substrate 220 via a plurality of first electrically conductive bumps 270 so as to cover the opening 222 of the substrate 220. Moreover, the lower chip 230 is accommodated in the opening 222 and attached to the upper chip 220 via a plurality of second electrically conductive bumps 280.

[0018] Furthermore, the heat spreader 250 is attached to the back surface 214 of the upper chip 210 through an adhesive layer 290 and is mounted on the dam 240 that is disposed between the substrate 220 and the lower surface 252 of the heat spreader 250. Therein, the adhesive layer 290 may be a thermally conductive epoxy so as to enhance thermal performance of the multi-chips stacked package. In addition, the dam 240

surrounds the upper chip 210. In such a manner, the dam 240, the heat spreader 250 and the upper surface 224 of the substrate 220 enclose a space 300 for filling with said underfill 260. Thus, the upper chip 210, the lower chip 230, the first electrically conductive bumps 270 and the second electrically conductive bumps 280 are enclosed by the underfill 260, and a portion of the substrate 220 is covered by said underfill 260 so as to have the underfill 260 connected to the heat spreader 250, the dam 240 and the upper surface 224 of the substrate 220. Accordingly, a reinforced structure comprising the underfill 260, the dam 240 and the heat spreader 250 is formed to restrain the deformation of the upper chip 210 and the warpage of the substrate 220 and to prevent the first electrically conductive bumps 270 from being damaged due to CTE mismatch of the substrate 220 with the upper chip 210. Moreover, a plurality of solder balls 228 are provide on the lower surface 226 of the substrate 220 so as to electrically connect to external electronic devices. It should be noted that the underfill may be replaced with another encapsulation, such as epoxy and plastic polymer.

[0019] As mentioned above, the dam 240 may be an adhesive body made of an epoxy or a thermally conductive epoxy, and is disposed on the upper surface 222 of the substrate 220 by dispensing method. Furthermore, the dam 240 surrounds the periphery of the chip 210, and is shaped into a ring as shown in FIG. 3 or four bars located at the four sides (not shown). Namely, the dam 240 encloses the upper chip 210 and prevents the underfill 260 from bleeding.

[0020] As mentioned above, when the thickness or the size of the upper chip 210 is larger than usual one, the heat spreader 250 can be made of a material with a coefficient of thermal expansion similar with the substrate 220. On the contrast, when the thickness or the size of the upper chip 210 is smaller than usual one, the heat spreader 250 can be made of a material with a coefficient of thermal expansion

similar with the chip. For example, a dummy chip is taken as a heat spreader. Because the coefficient of thermal expansion of the heat spreader 250 is ranged between the chip and the substrate and a reinforced structure is formed by the underfill 260, the dam 240 and the heat spreader 250, the warpage of the substrate 220 and the deformation of the upper chip 210 will be restrained to avoid the first electrically conductive bumps 270 connecting the upper chip 210 and the substrate 220 being damaged. It should be noted that the heat spreader 250 is a flat plate and the material of the heat spreader is made of copper or aluminum so that the thermal performance of the multi-chips stacked package will be enhanced. When the package is taken for communication and wire-less module application, a lead frame as lead-less lead frame, will replace the substrate.

[0021] Moreover, when the substrate 320 has no opening therein, the lower chip 230 will be placed above the upper surface 324 of the substrate 320 as shown in FIG. 4 which is taken as a second preferred embodiment. Accordingly, the height of the first electrically conductive bump 370 connecting the upper chip 310 to the substrate 320 is larger than that of the electrically conductive bump 380 connecting the lower chip 330 to the upper chip 310.

[0022] Although the invention has been described in considerable detail with reference to certain preferred embodiments, it will be appreciated and understood that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the appended claims.